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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,875	09/22/2003	Naoteru Matsubara	65933-044	4231

7590 12/15/2005

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
IM, JUNGHWA M	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,875	MATSUBARA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 11, 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh (US 6225207) in view of Gates et al. (US 6603204), hereinafter Gates.

Regarding claim 1, Fig. 4F of Parikh shows a semiconductor device comprising:

a semiconductor substrate [410];

a multilayered film including a first dielectric film [412, 416], an etching stopper [418] and a second dielectric film [420] stacked on said semiconductor substrate in this order; and

a via plug [452] and a metal interconnect [450] formed in said multilayered film;

wherein the upper surface of said etching stopper is located under the upper surface level of said metal interconnect and the under surface of said etching stopper is located over the under

surface level of said metal interconnect, and

wherein said metal interconnect is embedded in an area at least including a trench formed in the second dielectric film using the etching stopper.

Fig. 1F of Parikh shows substantially the entire claimed structure except "the dielectric constant of said etching stopper being larger than that of said first and second dielectric films." Fig. 8 of Gates shows a semiconductor device with a multilayered film [52'] including a first dielectric film [54'], an etching stopper [56'] and a second dielectric film [58'] stacked on said semiconductor substrate in this order, the dielectric constant of said etching stopper being larger than that of said first and second dielectric films (col. 4, lines 8-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Gates into the device of Parikh in order to have the dielectric constant of the etching stopper being larger than that of the first and second dielectric films to enhance the circuit speed of the integrated circuit (col. 1, lines 7-16).

Regarding claim 2, Gates discloses the semiconductor device wherein the dielectric constant [k=1.1-5.5] of said etching stopper is less than or equal to 5 [col. 4, lines 60-65].

Regarding claims 3 and 4, Gates discloses the semiconductor device wherein the dielectric constant of said etching stopper is larger than or equal to a summation of 2 and the dielectric constant of either one of the dielectric constants [k=1.4-3.5] of said first and second dielectric films [col. 4, lines 15-17].

Regarding claim 5, Gates discloses said metal interconnect includes copper as a constituting element [col. 7, lines 34-36].

Response to Arguments

Applicant's arguments filed October 11, 2005 have been fully considered but they are not persuasive.

Applicants argue that "... claim 1 ... wherein the upper surface of the etching stopper is located under the upper surface level of the metal interconnect and the under surface of the etching stopper is located over the under surface level of the metal interconnect and, moreover, the metal interconnect is embedded in an area at least including a trench formed in the second dielectric film using the etching stopper. No such structure is disclosed or suggested by Parikh." Examiner disagrees. Parikh shows very limitation recited in the claim 1 as fully discussed above in the office action.

Applicants further argue that "[i]ndeed, adverting to Fig. 4 of Parikh, the dielectric layer (414) functioning as an etching stopper defines the under surface of the metal interconnect (450). It is **not,** repeat **not,** the etching stopper (418) that defines the under surface of the metal interconnect (450). ... Again, the under surface of metal interconnect (450) is not defined by etching stopper (418)." It is pointed out that this aspect is not recited in the instant invention. Rather, claim 1 simply recites that "the upper surface of said etching stopper is located under the upper surface level of said metal interconnect and the under surface of said etching stopper is located over the under surface level of said metal interconnect." The metal interconnect 450 in Fig. 4 of Parikh reads on this limitation.

Applicants further argue that "... it should be apparent that even if the applied references are combined as suggested by the Examiner, and Applicants do **not** agree that the requisite fact-based motivation has been established, the claimed invention would **not** result."

Examiner disagrees. Fig. 4 of Parikh shows all the structural limitations in the instant invention. Gates is referred merely to meet the limitation on dielectric constant. Therefore, the combined teachings of Parikh and Gates would result in a device recited in the instant invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800